

DIALOG(R)File 345:Inpadoc/Fam.& Legal Stat

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Basic Patent (No,Kind,Date): JP 4273452 A2 19920929 <No. of Patents: 014>

METHOD OF MOUNTING IC CHIP (English)

Patent Assignee: SEMICONDUCTOR ENERGY LAB

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IPC: \*H01L-021/60; H01L-021/66; H01L-023/10

Derwent WPI Acc No: C 92-370823

JAPIO Reference No: 170069E000108

Language of Document: Japanese

Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date	
JP 4273452	A2	19920929	JP 9158324	A	19910228	(BASIC)
JP 4295090	A2	19921020	JP 9158825	A	19910322	
JP 4295091	A2	19921020	JP 9158826	A	19910322	
JP 4295092	A2	19921020	JP 9158827	A	19910322	
JP 5213694	A2	19930824	JP 9158824	A	19910322	
<b>JP 7014880</b>	A2	19950117	JP 9256783	A	19920207	
JP 2564728	B2	19961218	JP 9256783	A	19920207	
JP 3047485	B2	20000529	JP 9158824	A	19910322	
JP 3047486	B2	20000529	JP 9158825	A	19910322	
JP 3047487	B2	20000529	JP 9158826	A	19910322	
JP 3047488	B2	20000529	JP 9158827	A	19910322	
KR 9602093	B1	19960210	KR 923059	A	19920227	
<u>US 5261156</u>	A	19931116	US 841526	A	19920226	
US 5314540	A	19940524	US 855742	A	19920323	

Priority Data (No,Kind,Date):

JP 9158324 A 19910228

JP 9158825 A 19910322

JP 9158826 A 19910322

JP 9158827 A 19910322

JP 9158824 A 19910322

JP 9256783 A 19920207

JP 9158324 A1 19910228

DIALOG(R)File 347:JAPIO

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04694280 \*\*Image available\*\*

MOUNTING METHOD FOR CHIP OF SEMICONDUCTOR INTEGRATED CIRCUIT AND ELECTRONIC

EQUIPMENT MOUNTED THEREWITH

PUB. NO.: 07-014880 [JP 7014880 A]

PUBLISHED: January 17, 1995 (19950117)

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APPL. NO.: 04-056783 [JP 9256783]

FILED: February 07, 1992 (19920207)

INTL CLASS: [6] H01L-021/60; H01L-021/66

JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 46.2  
(INSTRUMENTATION -- Testing)

JAPIO KEYWORD: R011 (LIQUID CRYSTALS); R116 (ELECTRONIC MATERIALS -- Light Emitting Diodes, LED)

#### ABSTRACT

PURPOSE: To provide a COG type semiconductor integrated circuit chip mounting method wherein a defective chip can be replaced for repair.

CONSTITUTION: A semiconductor integrated circuit chip and a wiring are electrically connected together through the intermediary of projections (bumps) or conductive particles on the lead-out electrodes of the chip or the electrode wiring on a board, wherein organic resins different in setting condition such as photosetting, thermosetting, or naturally setting resin are combined and mixed together into an organic resin mixture, the resin mixture is used in a tentative bonding process, it is checked that a defective part is present or not, and a defective semiconductor integrated circuit is replaced with a new one by removing organic resin.